What is claimed is:

1. A spread-spectrum demodulator comprising:

a spreading code generating section which generates a spreading code for correlating with a received spread signal;

a correlation value computing section which computes a correlation value between the spread signal and the spreading code output from said spreading code generating section;

a data signal demodulating section which detects a peak of an output from said correlation value computing section and demodulates a data signal on the basis of the detected peak;

a peak signal detecting section which detects the peak of the output from said correlation value computing section; and

a spreading code generation control section which changes a shifting direction of the spreading code relative to the spread signal every time a peak is detected by said peak signal detecting section.

2. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal;

a sample/hold control circuit which receives a

first clock having the same frequency as that of a clock used to spread the baseband signal, and performs control to make said N sample/hold circuits sequentially perform sample/hold operation in synchronism with the first clock;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

N multipliers which multiply signals output from said sample/hold circuits and spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code

generating circuit to said multipliers every time the peak is detected by said peak detector.

3. A demodulator according to claim 2, wherein said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group, said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop

circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

4. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

N multipliers which multiply signals output from said sample/hold circuits and spreading codes output from said spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code

generating circuit in accordance with detection of the peak by said peak detector.

5. A demodulator according to claim 4, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

6. A demodulator according to claim 4, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

7. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a spreading code generating circuit which generates N spreading codes in synchronism with a second

clock;

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

8. A demodulator according to claim 7, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

9. A demodulator according to claim 7, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

10. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers every time the peak is detected by said peak detector.

11. A demodulator according to claim 10, wherein said register circuit comprises a flip-flop circuit,

said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a

second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

12. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal;

a sample/hold control circuit which receives a first clock having the same frequency as that of a clock used to spread the baseband signal, and performs control to make said N sample/hold circuits sequentially perform sample/hold operation in synchronism with the first clock;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

a polarity conversion circuit which outputs nearly half of the N spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the codes without any change,

N multipliers which multiply signals output from said sample/hold circuits and spreading codes output from said polarity conversion circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said polarity conversion circuit and inputting of the

second spreading codes from said second spreading code generating circuit to said polarity conversion circuit every time the peak is detected by said peak detector.

13. A demodulator according to claim 12, wherein said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group, said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a

first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

14. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal;

a sample/hold control circuit which receives a first clock having the same frequency as that of a clock used to spread the baseband signal, and performs control to make said N sample/hold circuits sequentially perform sample/hold operation in synchronism with the first clock;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

N multipliers which multiply signals output from said sample/hold circuits and spreading codes

output from said first spreading code generating circuit or said second spreading code generating circuit;

a polarity conversion circuit which outputs nearly half of multiplier output signals from said N multipliers which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change,

an adder which adds outputs from said polarity conversion circuit;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers every time the peak is detected by said peak detector.

15. A demodulator according to claim 14, wherein said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop

circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

16. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal;

a sample/hold control circuit which receives a first clock having the same frequency as that of a clock used to spread the baseband signal, and performs control to make said N sample/hold circuits sequentially perform sample/hold operation in synchronism with the first clock;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

a polarity conversion circuit which outputs nearly half of sample/hold output signals from said N sample/hold circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the sample/hold output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the sample/hold signals without any change,

N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers every time the peak is detected by said peak detector.

17. A demodulator according to claim 16, wherein said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop

circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

18. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal in synchronism with a first clock having the same frequency as that of a clock used to

spread the baseband signal;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

a polarity conversion circuit which outputs nearly half of the N spreading codes output from said spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the codes without any change;

N multipliers which multiply signals output from said sample/hold circuits and spreading codes output from said polarity conversion circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

19. A demodulator according to claim 18, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

20. A demodulator according to claim 19, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

21. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

N multipliers which multiply signals output from said sample/hold circuits and spreading codes output from said spreading code generating circuit for each corresponding signal;

a polarity conversion circuit which outputs nearly half of the multiplier output signals from said N

multipliers which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change;

an adder which adds outputs from said polarity conversion circuit;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

22. A demodulator according to claim 21, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

23. A demodulator according to claim 21, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected

by said peak detector.

24. A spread-spectrum demodulator comprising:

N (N is an integer not less than 2) sample/hold circuits each of which samples/holds a received spread signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

a polarity conversion circuit which outputs nearly half of the sample/hold output signals from said N sample/hold circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the sample/hold output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the sample/hold output signals without any change;

N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an

output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

25. A demodulator according to claim 24, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

26. A demodulator according to claim 24, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

27. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit

by one period to (N - 1) periods of the first clock, respectively;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

a polarity conversion circuit which outputs nearly half of the N spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the codes without any change,

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on

the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said polarity conversion circuit and inputting of the second spreading codes from said second spreading code generating circuit to said polarity conversion circuit every time the peak is detected by said peak detector.

28. A demodulator according to claim 27, wherein

said register circuit comprises a flip-flop circuit,

said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first

spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

29. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a first spreading code generating circuit which generates N first spreading codes in synchronism

with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock;

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said first spreading code generating circuit or said second spreading generating circuit for each corresponding signal;

a polarity conversion circuit which outputs nearly half of the multiplier output signals from said N multipliers which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change,

an adder which adds outputs from said polarity conversion circuit;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit

to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers time the peak is detected by said peak detector.

30. A demodulator according to claim 29, wherein said register circuit comprises a flip-flop circuit,

said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which

openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

31. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order

in synchronism with the second clock;

a polarity conversion circuit which outputs nearly half of output signals from said comparator circuit and said register circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the output signals without any change,

N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said first spreading code generating circuit or said second spreading generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers time the peak is detected by said peak detector.

32. A demodulator according to claim 31, wherein said register circuit comprises a flip-flop circuit,

said first spreading code generating circuit comprises N flip-flop circuits of a first flip-flop circuit group each of which shifts the first spreading code in synchronism with the second clock, a first exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits of said first flip-flop circuit group, and a first switch group which openably cascades the flip-flop circuits of said first flip-flop circuit group and openably connects an output of said first exclusive-OR circuit to an input of a first-stage flip-flop circuit in said first flip-flop circuit group,

said second spreading code generating circuit comprises N flip-flop circuits of a second flip-flop circuit group each of which shifts the second spreading code in a reverse direction relative to the first spreading code in synchronism with the second clock, a second exclusive-OR circuit which receives outputs from a plurality of flip-flop circuits in said second flip-flop circuit group, and a second switch group which openably cascades the flip-flop circuits of said second flip-flop circuit group and openably connects an output of said second exclusive-OR circuit to an input of a first-stage flip-flop circuit in said second flip-flop

circuit group, and

said spreading code control circuit which alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the peak is detected by said peak detector.

33. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

a polarity conversion circuit which outputs nearly half of N spreading codes output from said spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period

of the second clock, and outputs remaining nearly half of the codes without any change,

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said polarity conversion circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

34. A demodulator according to claim 33, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

35. A demodulator according to claim 33, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

36. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

N multipliers which multiply signals output from said comparator circuit and said register circuits and spreading codes output from said spreading code generating circuit for each corresponding signal;

a polarity conversion circuit which outputs nearly half of multiplier output signals from said N multipliers which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change,

an adder which adds outputs from said polarity conversion circuit;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

37. A demodulator according to claim 36, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

38. A demodulator according to claim 36, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

39. A spread-spectrum demodulator comprising:

a comparator which converts a received spread signal into a digital signal in synchronism with a first clock having the same frequency as that of a clock used to spread the baseband signal;

(N - 1) (N is an integer not less than 2) register circuits which output (N - 1) signals by delaying an output signal from said comparator circuit by one period to (N - 1) periods of the first clock, respectively;

a spreading code generating circuit which generates N spreading codes in synchronism with a second clock;

a polarity conversion circuit which outputs nearly half of output signals from said comparator circuit and said sample/hold circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the output signals without any change,

N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said spreading code generating circuit for each corresponding signal;

an adder which adds outputs from said N multipliers;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a clock control circuit which controls

inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector.

40. A demodulator according to claim 39, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector.

41. A demodulator according to claim 39, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined period of time when the peak is detected by said peak detector.

42. A demodulator according to claim 3, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

43. A demodulator according to claim 42, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

44. A demodulator according to claim 42, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

45. A demodulator according to claim 11, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the

respective flip-flop circuits of said first flip-flop circuit group.

46. A demodulator according to claim 45, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

47. A demodulator according to claim 45, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

48. A demodulator according to claim 13, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop

circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

49. A demodulator according to claim 48, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

50. A demodulator according to claim 48, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

51. A demodulator according to claim 15, wherein inputs of the respective flip-flop circuits of said

first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

52. A demodulator according to claim 51, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

53. A demodulator according to claim 51, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

54. A demodulator according to claim 17, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

55. A demodulator according to claim 54, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

56. A demodulator according to claim 54, wherein

said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

57. A demodulator according to claim 28, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

58. A demodulator according to claim 57, wherein

said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control

signal is output.

59. A demodulator according to claim 57, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

60. A demodulator according to claim 30, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

61. A demodulator according to claim 60, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit

alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

62. A demodulator according to claim 60, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

63. A demodulator according to claim 32, wherein inputs of the respective flip-flop circuits of said first flip-flop circuit group excluding the first-stage flip-flop circuit, are connected to inputs of the respective flip-flop circuits of said second flip-flop circuit group excluding the first-stage flip-flop circuit, for each corresponding circuit, to output the first spreading codes or second spreading codes from the respective flip-flop circuits of said first flip-flop circuit group.

64. A demodulator according to claim 63, wherein said peak detector comprises means for determining a reference level from a peak level of an output from said adder and a predetermined lower limit level, and means for comparing the reference level with an output from said adder to generate a control signal

synchronized with a trailing edge of a peak signal of an output from said adder, and

said spreading code control circuit alternately switches control operation of turning on said first switch group and control operation of turning on said second switch group every time the control signal is output.

65. A demodulator according to claim 63, wherein said peak detector comprises means for determining the lower limit level on the basis of a power supply voltage and a common mode level.

66. A demodulator according to claim 1, further comprising a filter which passes only a signal component, of a signal output from said data signal demodulating section, which falls within a data frequency band.

67. A demodulator according to claim 1, further comprising demodulation means for demodulating a data signal by counting peaks of outputs from said correlation value computing section in place of said data signal demodulating section.